CLAIMS

1. *(ORIGINAL)* An apparatus including a metal oxide semiconductor (MOS) bandgap voltage reference circuit, comprising:

MOS bandgap voltage generator circuitry including

first and second parasitic substrate transistor circuits with first and second base terminals, first and second emitter terminals, first and second collector terminals, and first and second emitter areas, respectively, and

a first resistance coupled between said first and second base terminals,

wherein said first emitter area is greater than said second emitter area and one of said first emitter and collector terminals is mutually coupled with a like one of said second emitter and collector terminals; and

a plurality of dummy transistors with mutually coupled base terminals coupled to said second base terminal, and mutually coupled emitter terminals and mutually coupled collector terminals coupled to said mutually coupled first and second parasitic substrate transistor circuit terminals.

2. *(ORIGINAL)* The apparatus of claim 1, wherein each one of at least a portion of said plurality of dummy transistors has an emitter area substantially equal to said second emitter area.

3. *(ORIGINAL)* The apparatus of claim 1, further comprising startup circuitry coupled to said MOS bandgap voltage generator circuitry and responsive to an application of power to said MOS bandgap voltage generator circuitry by initiating first and second currents in said first and second parasitic substrate transistor circuits, respectively.

4. *(ORIGINAL)* The apparatus of claim 1, wherein said MOS bandgap voltage generator circuitry comprises:

MOS current source circuitry including a control terminal and first, second, third and fourth output terminals, and responsive to a control signal by providing an output voltage via said first output terminal, substantially equal first and second source currents via said second and third output terminals, and first and second source voltages via said third and fourth output terminals;

said first parasitic substrate transistor circuit coupled to said second output terminal;

said second parasitic substrate transistor circuit coupled to said third output terminal;

amplifier circuitry coupled to said third and fourth output terminals and said control terminal, and responsive to said first and second source voltages by providing said control signal; and

resistive circuitry coupled to said first output terminal, said second base terminal and said mutually coupled first and second parasitic substrate transistor circuitry terminals.

5. *(ORIGINAL)* The apparatus of claim 4, wherein said MOS current source circuitry comprises:

a MOS transistor coupled to said control terminal and said first output terminal;

a second resistance coupled to said first output terminal;

third and fourth resistances coupled to said second resistance and said third and fourth output terminals; and

a fifth resistance coupled to said second and fourth output terminals.

6. *(ORIGINAL)* The apparatus of claim 4, wherein:

said first parasitic substrate transistor circuit comprises a first plurality of bipolar junction transistors;

said second parasitic substrate transistor circuit comprises a second plurality of bipolar junction transistors, wherein said first and second collector terminals are mutually coupled;

said first and second pluralities of bipolar junction transistors are integrated in a substantially symmetrical first array having a periphery; and

said plurality of dummy transistors are integrated in a second array substantially adjacent at least a portion of said periphery.

7. *(ORIGINAL)* The apparatus of claim 4, wherein:

said first parasitic substrate transistor circuit comprises a first plurality of PNP bipolar junction transistors; and

said second parasitic substrate transistor circuit comprises a second plurality of PNP bipolar junction transistors, wherein said first and second collector terminals are mutually coupled.

8. *(ORIGINAL)* The apparatus of claim 4, wherein said amplifier circuitry comprises a differential amplifier circuit with first and second amplifier input terminals coupled to said third and fourth output terminals, respectively, and an amplifier output terminal coupled to said control terminal.

9. *(ORIGINAL)* The apparatus of claim 4, wherein said resistive circuitry comprises:

a second resistance coupled to said first output terminal and said second base terminal; and

a third resistance coupled to said second base terminal and said mutually coupled first and second parasitic substrate transistor circuitry terminals.

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